CARL FORD

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EXPERIENCED DIGITAL DESIGNER / ENGINEER

Seasoned professional with degree in engineering / computer science and 15+ award-winning and patent-filled years of experience in mainframe computer hardware and software design engineering. Proven ability to resolve complex technical roadblocks through phases including system design, new hardware bring up, and debug in complex digital logic design and micro code programming projects. Known for delivering top quality, innovative designs on time and error free. Demonstrated track record of quickly and easily mastering new concepts, designs, programming languages, tools, and architectures to achieve goals. Expertise in VHDL, Perl, Cadence. Open to travel and relocation.

TECHNICAL EXPERIENCE

Software:	Cadence (12 years, Skill: Expert), Adobe Frame Maker / Photoshop / Acrobat, Microsoft Word / Excel / PowerPoint / Project
OS:	Client Server & Mainframe – Windows 9X / NT / 2000 / XP, AIX / UNIX, Linux, VM/CMS, SAK, z/OS
Programming:	VHDL, Perl, Cadence Skill, C, HTML, PLX, PLAS, Rexx, 370 Assembler, CMS Pipelines, Pascal, LISP, APL
Architecture:	Exceptional grasp of complex architecture areas like interrupt handling, page tables, I/O
Debugging:	Software & hardware QA / QC / problem determination & resolution, interactive debug & dump analysis, extensive new system bring up and test floor experience

PROFESSIONAL EXPERIENCE

IBM HARDWARE PHYSICAL DESIGN TOOLS, 11/05 to Present

Advisory Engineer (Interim Assignment)

- Tasked with aiding Hardware Physical Design Tools Team in solving persistent integration problems in tape out of current IBM mainframe server. Research and apply technology and best approaches.
- Lead definition, design and implementation of new methodology for buffer optimization tool to automate integration timing closure.
- Work with team to define / implement methodology for synchronous latch staging in multiple hierarchies.
- Work with team to define and implement new methodology for synchronous latch clustering.

SELECTED ACCOMPLISHMENTS

- Firmed up open-ended definitions and ideas, defined previously stalled user interface, and designed and implemented code to fill 'holes' immediately.
- Finished 32 mini-programming projects using Perl and Cadence Skill languages to resolve complex design and performance issues.

IBM S/390 DIVISION HARDWARE POWER ON, 11/03 to 11/05.

Technical Leader

- Appointed as hands-on leader of large systems running stress, architecture, and real world test cases for IBM z9-109 mainframe server in initial Hardware Power On and Bring Up Team.
- Assessed daily progress and reallocated resources and priorities to keep projects running on track.
- Served as on-the-spot resource, listening to and analyzing problems, recommending workarounds, and directing team to sustain focus and on-time status toward GA.
- Used broad hardware and software knowledge (CEC hardware, IO hardware, microcode, and operating systems) and grasp of other teams' needs (function test, recovery test, technology test, performance test, etc.) to enable Bring Up team to accomplish missions on time.

SELECTED ACCOMPLISHMENTS

- Found over 50% of problems; isolated problems to failing test cases, collected debug data, and successfully tested new hardware and software.
- gathering debug data, new problem discovery, installing new hardware, installing updated software, user requests for debug time, and available personnel.
- Designed / implemented new bring up tools in Perl and Rexx and enhanced existing tools and debug data infrastructure and web server to significantly increase speed and accuracy of test process.
- Led Bring Up team's switch from OS2 to Linux-based tools and provided Linux SE training and support.

IBM S/390 DIVISION CMOS CHIP DESIGN, 10/93 to 11/03
Chip Designer

- Promoted through numerous design engineering roles to serve as primary logic designer for Level 2 Cache Controller Chips used in IBM G4, G5, G6, z900, z990 and z9-109 CMOS mainframes.
- Managed all aspects of design and high-level schematics and VHDL in Cadence, partitioned and road-mapped logic, resolved simulation problems, evaluated new function and change requests.
- Created and implemented Key Cache, Central Priority, Central Pipeline, Recovery, Environmentals, Configuration Array and Trace logic.
- Synthesized or hand-designed logic and optimized number of circuits, wiring, pins, power and timing.
- Served as Logic Coordinator, Integrator, and Co-leader for G4 G5, G6, z900 and z990 chips.
- Coordinated, established and tracked checkpoints, by developing and refining the chip schematic and resolving interface problems.

SELECTED ACCOMPLISHMENTS

- Recognized for error-free designs that exceed requirements within schedule.
- Reduced design time and complexity by establishing conventions and nomenclature for chips.
- Spearheaded writing of G4 workbook contributed major portion of G5, G6, z900 and Z990 workbooks.
- Played key role in on-schedule chip release by finding / filling holes in chip design tools & methodology.
- Quickly taught myself Perl and Cadence Skill programming and wrote many outstanding tools for team.
- Created Turbo VHDL and Turbo Schematic VHDL macro language, fast VHDL netlister, fast IBM Synthesis import, and cone of logic tracer, which significantly enhanced productivity by reducing time to code VHDL by greatly reducing required code writing and eliminating errors before simulation.

IBM ES/9000 BIPOLAR CHIP / MCM DESIGN, 2/89 to 10/93.
Chip Logic Designer / Engineer

- Provided chip logic design for Level 2 Cache Controller chips for IBM ES/9000 mainframe.
- Developed and implemented cache fetch and store controls, with logic implemented on 6 bipolar chips.
- Responsible for all aspects of design: coordinated efforts of 14 chip designers working on 127-mm MCM with 115 chips.
- Established and tracked checkpoints, developed floor plan, resolved interface problems, and engineered valid net solutions.
- Orchestrated MCM timing analysis and numerous early design checks performed by team members.

IBM PROCESSOR CONTROLLER MICROCODE DEVELOPMENT, 6/83 to 2/89
Programmer & Associate Engineer

- Provided diverse programming, design engineering, and debugging services for varied mainframes.
- Named Project Leader for Logic Support Station Access Method.
- Developed entire design, gathered requirements, created documentation, implemented code, performed test and provided support and participated in four system bring ups.

EDUCATION

BS, Electrical Engineering / Computer Science, RUTGERS UNIVERSITY College of Engineering. 1983

PATENTS

Memory Management for a Symmetric Multiprocessor Computer System, US Patent #US7085897 (2006)
Programmable Hardware Event Monitoring Method, US Patent #6134676 (2000)
Computer Architecture Incorporating Processor Clusters and Hierarchical Cache Memories, US Patent #5752264 (1998)

AWARDS

IBM Outstanding Technical Achievement Award for "zSeries 20-way SMP" (2001)
IBM Outstanding Technical Achievement Award for "S/390 G5 Cache & Memory Development" (1998)
IBM Outstanding Technical Achievement Award for "S/390 G4 L2 Cache Development" (1997)
IBM First Patent Achievement Award for "Hierarchical Data Ownership on New System Structure" (1995)
IBM Outstanding Technical Achievement Award for "ES/9000 H5 Board Noise Support" (1992)

ASSOCIATIONS

Institute of Electrical and Electronics Engineers (IEEE), Six meetings per year. Tau Beta Pi